CLAIMS

1. A semiconductor member comprising:

a porous semiconductor layer which is made of a strain induction material on a semiconductor substrate; and

a strained semiconductor layer which is formed on the porous semiconductor layer.

2. The semiconductor member according to claim 1, wherein the strain induction material is SiGe.

3. The semiconductor member according to claim 1, further comprising a porous semiconductor layer made of the same material as the semiconductor substrate between the semiconductor substrate and said porous semiconductor layer made of the strain induction material.

4. A semiconductor member manufacturing method comprising:

a first step of porosifying a semiconductor layer containing a strain induction material on a semiconductor substrate to form a strain induction porous semiconductor layer; and

a second step of forming a strained semiconductor layer on the strain induction porous semiconductor layer.

5. The semiconductor member manufacturing method according to claim 4, wherein the first step comprises a step of, after the strain induction porous

semiconductor layer is formed, executing porosification by anodizing to relax an intrinsic lattice strain in the strain induction porous semiconductor layer.

6. The semiconductor member manufacturing method according to claim 4, wherein the first step comprises a step of, after the strain induction porous semiconductor layer is formed, executing annealing to relax an intrinsic lattice strain in the strain induction porous semiconductor layer.

7. A semiconductor member manufacturing method comprising:

a first step of porosifying a semiconductor layer containing a strain induction material on a semiconductor substrate to form a strain induction porous semiconductor layer;

a second step of stacking a strain induction material on the strain induction porous semiconductor layer to form a strain induction semiconductor layer; and

a third step of forming a strained semiconductor layer on the strain induction semiconductor layer.

8. The semiconductor member manufacturing method according to claim 4, wherein the strain induction material contains silicon and an additional material, and the additional material is a material different from silicon which is selected from the group consisting of germanium, a material containing gallium

and arsenic, a material containing gallium and phosphorus, and a material containing gallium and nitrogen.

9. The semiconductor member manufacturing method according to claim 4, wherein the first step comprises a stacking step of stacking the semiconductor layer containing the strain induction material on the substrate, and a porosification step of porosifying the semiconductor layer to form the strain induction porous semiconductor layer.

10. The semiconductor member manufacturing method according to claim 4, wherein the strain induction porous semiconductor layer is formed by porosifying the semiconductor layer containing the strain induction material by using anodizing.

11. The semiconductor member manufacturing method according to claim 4, wherein simultaneously as the semiconductor layer containing the strain induction material is porosified, the semiconductor substrate under an interface between the semiconductor substrate and the semiconductor layer containing the strain induction material is porosified to form a porous semiconductor layer.

12. The semiconductor member manufacturing method according to claim 4, wherein the semiconductor layer containing the strain induction material and the strained semiconductor layer are formed by CVD.

13. The semiconductor member manufacturing method according to claim 4, wherein the semiconductor layer containing the strain induction material is continuously formed in a CVD step while changing one of a flow rate and a concentration of a source gas to supply the strain induction material gradually or stepwise.

14. A semiconductor member manufacturing method comprising:

a step of preparing a first member obtained by forming an insulating layer on a strained semiconductor layer of a semiconductor member manufactured by using a manufacturing method of claim 4; and

a transfer step of transferring the insulating layer and the strained semiconductor layer from the first member to a second member after the first member and the second member are bonded so as to locate the insulating layer inside.

15. A semiconductor member manufacturing method comprising steps of:

preparing a first member including a semiconductor member manufactured by a manufacturing method of claim 4; and

bonding the first member to a second member which has at least a surface made of an insulating material so as to locate the strained semiconductor layer of the first member inside and transferring the strained

semiconductor layer from the first member to the second member.

16. The semiconductor member manufacturing method according to claim 14, wherein the transfer step is executed by separating the members at a strain induction porous semiconductor layer.

17. The semiconductor member manufacturing method according to claim 14, wherein the separation is done in a strain induction porous semiconductor layer, in a porous semiconductor layer formed by porosifying a semiconductor substrate, or in an interface between the strain induction porous semiconductor layer and one of the semiconductor substrate and the porous semiconductor layer formed by porosifying the semiconductor substrate.

18. The semiconductor member manufacturing method according to claim 14, wherein the separation is done at a defect generation portion in an interface between a strain induction porous layer and a porous semiconductor layer formed by porosifying a semiconductor substrate.

19. A semiconductor device having a transistor formed on a strained semiconductor layer of a semiconductor member of claim 1.

20. A semiconductor member comprising:

a first porous semiconductor layer which is made of a strain induction material on a semiconductor

substrate;

a second porous semiconductor layer which is formed on the first porous semiconductor layer; and

a strained semiconductor layer which is formed on the second porous semiconductor layer.

21. The semiconductor member according to claim 20, further comprising, between said second porous semiconductor layer and said strained semiconductor layer, a semiconductor layer which is made of the same material as the strain induction material.

22. The semiconductor member according to claim 20, wherein the strain induction material is SiGe.

23. The semiconductor member according to claim 20, wherein the material of said second porous semiconductor layer is one of Si and SiGe.

24. The semiconductor member according to claim 20, wherein said first porous semiconductor layer has lattice relaxation.

25. The semiconductor member according to claim 20, further comprising a third porous semiconductor layer made of the same material as the semiconductor substrate between the semiconductor substrate and said first porous semiconductor layer made of the strain induction material.

26. A semiconductor member manufacturing method comprising:

a first step of stacking a first semiconductor

layer containing a strain induction material on a semiconductor substrate, and a second semiconductor layer on the first semiconductor layer;

a second step of porosifying the first semiconductor layer containing the strain induction material and the second semiconductor layer to form a first porous semiconductor layer made of the strain induction material and a second porous semiconductor layer; and

a third step of forming a strained semiconductor layer on the second porous semiconductor layer.

27. A semiconductor member manufacturing method comprising:

a first step of stacking a first semiconductor layer containing a strain induction material on a semiconductor substrate, and a second semiconductor layer on the first semiconductor layer;

a second step of porosifying the first semiconductor layer containing the strain induction material and the second semiconductor layer to form a first porous semiconductor layer made of the strain induction material and a second porous semiconductor layer; and

a third step of stacking a semiconductor layer made of the same material as the strain induction material and a strained semiconductor layer on the second porous semiconductor layer.

28. The semiconductor member manufacturing method according to claim 26, wherein the strain induction material contains silicon and an additional material, and the additional material is a material different from silicon which is selected from the group consisting of germanium, a material containing gallium and arsenic, a material containing gallium and phosphorus, and a material containing gallium and nitrogen.

29. The semiconductor member manufacturing method according to claim 26, wherein the first porous semiconductor layer made of the strain induction material and the second porous semiconductor layer are formed by porosifying the first semiconductor layer containing the strain induction material and the second semiconductor layer stacked on the first semiconductor layer by using anodizing.

30. The semiconductor member manufacturing method according to claim 26, wherein simultaneously as the first semiconductor layer containing the strain induction material and the second semiconductor layer are porosified, the semiconductor substrate under an interface between the semiconductor substrate and the first semiconductor layer containing the strain induction material is porosified to form a third porous semiconductor layer.

31. The semiconductor member manufacturing method

according to claim 26, wherein the first semiconductor layer containing the strain induction material, the second semiconductor layer, and the strained semiconductor layer are formed by CVD.

32. The semiconductor member manufacturing method according to claim 26, wherein the first semiconductor layer containing the strain induction material is continuously formed in a CVD step while changing one of a flow rate and a concentration of a source gas to supply the strain induction material gradually or stepwise.

33. A semiconductor member manufacturing method comprising:

a step of preparing a first member obtained by forming an insulating layer on a strained semiconductor layer of a semiconductor member manufactured by using a manufacturing method of claim 26; and

a transfer step of transferring the insulating layer and the strained semiconductor layer from the first member to a second member after the first member and the second member are bonded so as to locate the insulating layer inside.

34. A semiconductor member manufacturing method comprising steps of:

preparing a first member including a semiconductor member manufactured by a manufacturing method of claim 26; and

bonding the first member to a second member which has at least a surface made of an insulating material so as to locate the strained semiconductor layer of the first member inside and transferring the strained semiconductor layer from the first member to the second member.

35. The semiconductor member manufacturing method according to claim 33, wherein the transfer step is executed by separating the members at a first porous semiconductor layer made of a strain induction material.

36. The semiconductor member manufacturing method according to claim 33, wherein the separation is done in a first porous semiconductor layer made of a strain induction material, in a third porous semiconductor layer formed by porosifying a semiconductor substrate, or in an interface between the first porous semiconductor layer made of the strain induction material and one of the semiconductor substrate and the third porous semiconductor layer formed by porosifying the semiconductor substrate.

37. The semiconductor member manufacturing method according to claim 33, wherein the separation is done at a defect generation portion in an interface between a first porous layer made of a strain induction material and a third porous semiconductor layer formed by porosifying a semiconductor substrate.

38. A semiconductor device having a transistor formed in a strained semiconductor layer of a semiconductor member of claim 20.